1.-16. (canceled)

17. (new) An apparatus comprising:

circuitry for sending and receiving serial input/output data at a rate equal to that of a source clock signal;

an instruction decoder connected to said circuitry for controlling the operation of said apparatus based on the decoding of a specific instruction;

a memory for storing instructions connected to said instruction decoder;

a program counter connected to said memory and to said instruction decoder; and

a function clock generator for generating a function clock signal that governs the rate of instruction execution within said apparatus, wherein said function clock generator is connected to said program counter, said instruction decoder, and said circuitry, and wherein the frequency of said function clock signal is decreased to equal the frequency of said source clock signal upon the decoding of said specific instruction.

18. (new) The apparatus of claim 17 wherein the decoding of said specific instruction causes said circuitry to send one bit of serial data.

19. (new) The apparatus of claim 17 wherein the decoding of said specific instruction causes said circuitry to receive one bit of serial data.

20. (new) The apparatus of claim 17 further comprising a repeat counter for receiving a count value indicating the number of times that the execution of said specific instruction is to be repeated.

21. (new) The apparatus of claim 20 wherein the repetitive execution of said specific instruction occurs at a rate equal to the source clock signal frequency.

22. (new) The apparatus of claim 20 wherein the repetitive execution of said specific instruction occurs over a predetermined number of bit cells.

23. (new) The apparatus of claim 17 wherein said specific instruction is encoded using no more than eight bits.

24. (new) A method comprising:

sending and receiving serial input/output data under the control of decoded instructions, and at a rate equal to the frequency of a source clock signal;

executing said instructions at a rate equal to that of the frequency of a function clock signal; and

decreasing the frequency of said function clock signal to be equal to the source clock signal, based on said decoded instructions.

25. (new) The method of claim 24 further comprising causing the sending or receiving of a single bit as a result of decoding an instruction.

26. (new) The method of claim 24 further comprising repeating the execution of an instruction over a predetermined number of bit cells at a rate equal to that of the source clock.

27. (new) The method of claim 24 further comprising decoding and executing a delay instruction, thereby causing a delay in the further execution of instructions for a number of cycles of the function clock signal specified in a count field, wherein said delay is achieved by asserting an alternate inhibit signal so as to temporarily reduce the frequency of the function clock signal.